

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

**TC74HC245AP, TC74HC245AF, TC74HC245AFW
TC74HC640AP, TC74HC640AF**

OCTAL BUS TRANSCEIVER

TC74HC245AP / AF / AFW 3— STATE, NON—INVERTING
TC74HC640AP / AF 3— STATE, INVERTING

(Note) The JEDEC SOP (FW) is not available in Japan.

The TC74HC245A, 640A are high speed CMOS OCTAL BUS TRANSCEIVERS fabricated with silicon gate C²MOS technology.

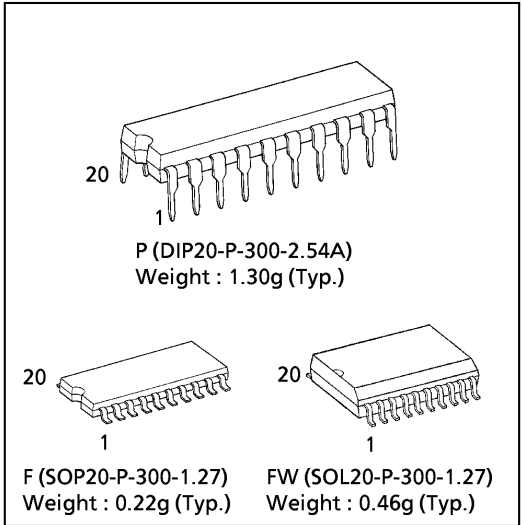
They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. They are intended for two-way asynchronous communication between data busses. The direction of data transmission is determined by the level of the DIR input.

The enable input (\bar{G}) can be used to disable the device so that the busses are effectively isolated.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES :

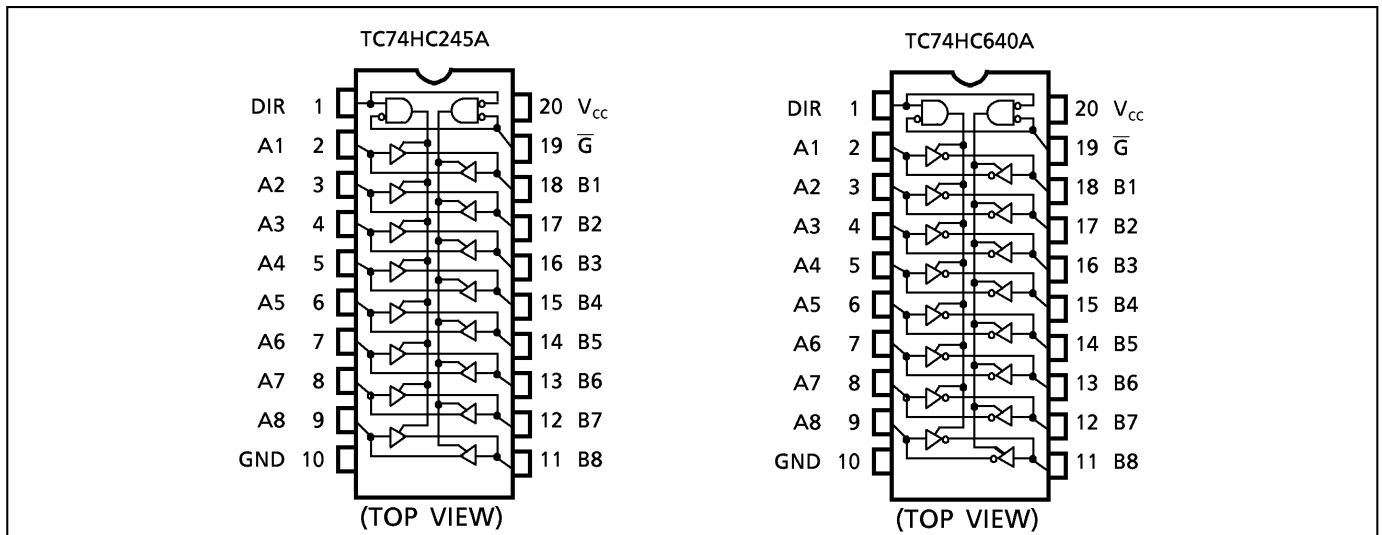
- High Speed..... $t_{pd} = 10ns$ (typ.) at $V_{CC} = 5V$
- Low Power Dissipation..... $I_{CC} = 4\mu A$ (Max.) at $T_a = 25^\circ C$
- High Noise Immunity..... $V_{NIH} = V_{NIL} = 28\% V_{CC}$ (Min.)
- Output Drive Capability..... 15 LSTTL Loads
- Symmetrical Output Impedance... $|I_{OH}| = I_{OL} = 6mA$ (Min.)
- Balanced Propagation Delays..... $t_{pLH} \approx t_{pHL}$
- Wide Operating Voltage Range... V_{CC} (opr.) = 2V~6V
- Pin and Function Compatible with 74LS 245 / 640



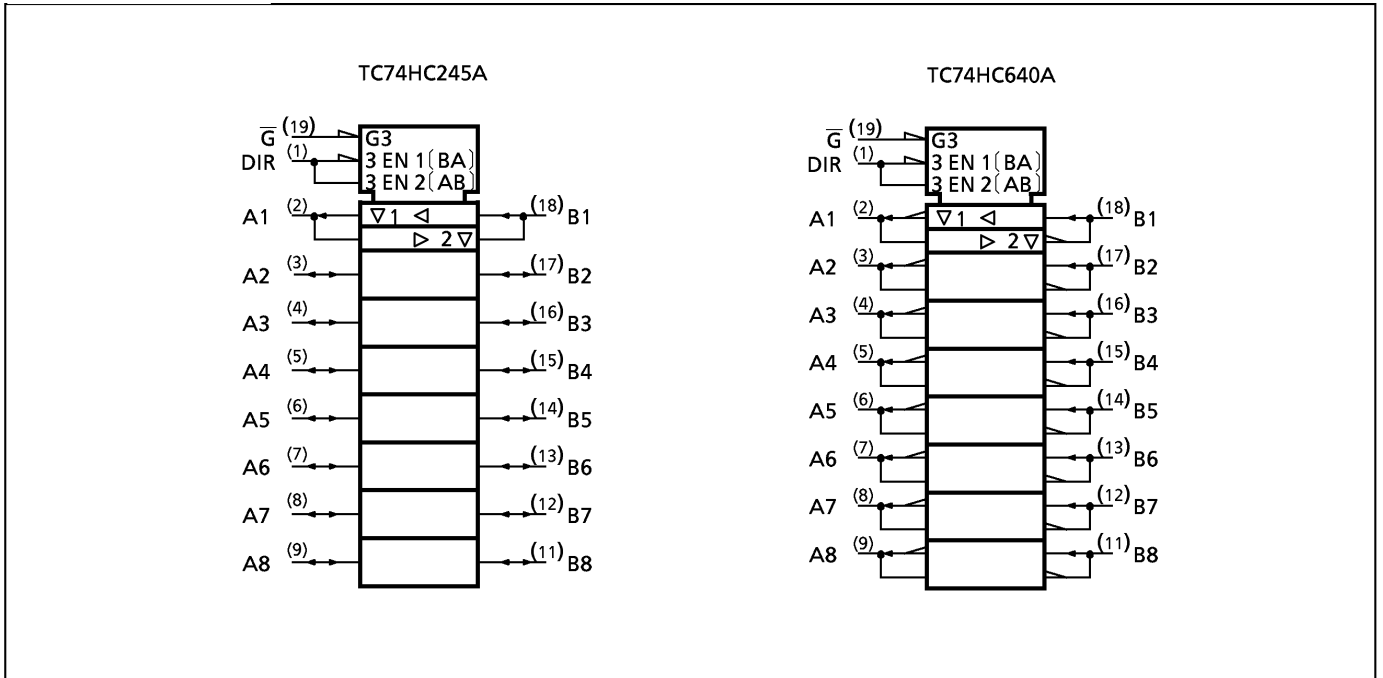
APPLICATION NOTES

- 1) Do not apply a signal to any bus terminal when it is in the output mode. Damage may result.
- 2) All floating (high impedance) bus terminals must have their input levels fixed by means of pull up or pull down resistors.

PIN ASSIGNMENT



IEC LOGIC SYMBOL



TRUTH TABLE

INPUTS		FUNCTION		OUTPUTS	
\bar{G}	DIR	A BUS	B BUS	HC245A	HC640A
L	L	OUTPUT	INPUT	$A = B$	$A = \bar{B}$
L	H	INPUT	OUTPUT	$B = A$	$B = \bar{A}$
H	X	High Impedance		Z	Z

X : "H" or "L"
Z : High Impedance

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5~7	V
DC Input Voltage	V_{IN}	-0.5~ $V_{CC} + 0.5$	V
DC Output Voltage	V_{OUT}	-0.5~ $V_{CC} + 0.5$	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC} / Ground Current	I_{CC}	±75	mA
Power Dissipation	P_D	500 (DIP)* / 180 (SOP)	mW
Storage Temperature	T_{stg}	-65~150	°C

*500mW in the range of $T_a = -40^{\circ}\text{C} \sim 65^{\circ}\text{C}$. From $T_a = 65^{\circ}\text{C}$ to 85°C a derating factor of $-10\text{mW}/^{\circ}\text{C}$ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2~6	V
Input Voltage	V_{IN}	0~ V_{CC}	V
Output Voltage	V_{OUT}	0~ V_{CC}	V
Operating Temperature	T_{opr}	-40~85	°C
Input Rise and Fall Time	t_r, t_f	0~1000 ($V_{CC} = 2.0\text{V}$) 0~500 ($V_{CC} = 4.5\text{V}$) 0~400 ($V_{CC} = 6.0\text{V}$)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	$T_a = 25^{\circ}\text{C}$			$T_a = -40 \sim 85^{\circ}\text{C}$		UNIT	
				MIN.	TYP.	MAX.	MIN.	MAX.		
High - Level Input Voltage	V_{IH}		2.0	1.50	—	—	1.50	—	V	
			4.5	3.15	—	—	3.15	—		
			6.0	4.20	—	—	4.20	—		
Low - Level Input Voltage	V_{IL}		2.0	—	—	0.50	—	0.50	V	
			4.5	—	—	1.35	—	1.35		
			6.0	—	—	1.80	—	1.80		
High - Level Output Voltage	V_{OH}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -20\mu\text{A}$	2.0	1.9	2.0	—	1.9	—	V
				4.5	4.4	4.5	—	4.4	—	
				6.0	5.9	6.0	—	5.9	—	
Low - Level Output Voltage	V_{OL}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 20\mu\text{A}$	2.0	—	0.0	0.1	—	0.1	V
				4.5	—	0.0	0.1	—	0.1	
				6.0	—	0.0	0.1	—	0.1	
3 - State Output Off - State Current	I_{OZ}	$V_{IN} = V_{IH}$ or V_{IL} $V_{OUT} = V_{CC}$ or GND	6.0	—	—	±0.5	—	±5.0	μA	
Input Leakage Current	I_{IN}	$V_{IN} = V_{CC}$ or GND	6.0	—	—	±0.1	—	±1.0	μA	
Quiescent Supply Current	I_{CC}	$V_{IN} = V_{CC}$ or GND	6.0	—	—	4.0	—	40.0		

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 6\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITION	CL (pF)	V _{CC} (V)	Ta = 25°C			Ta = -40~85°C		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		50	2.0	—	52	60	—	75	ns
				4.5	—	7	12	—	15	
				6.0	—	6	10	—	13	
Propagation Delay Time	t_{pLH} t_{pHL}		50	2.0	—	33	90	—	115	
				4.5	—	12	18	—	23	
				6.0	—	10	15	—	20	
			150	2.0	—	48	120	—	150	
				4.5	—	16	24	—	30	
				6.0	—	14	20	—	26	
3 -State Output Enable time	t_{pZL} t_{pZH}	$R_L = 1\text{k}\Omega$	50	2.0	—	48	150	—	190	
				4.5	—	16	30	—	38	
				6.0	—	14	26	—	32	
			150	2.0	—	63	180	—	225	
				4.5	—	21	36	—	45	
				6.0	—	18	31	—	38	
3 -State Output Disable time	t_{pLZ} t_{pHZ}	$R_L = 1\text{k}\Omega$	50	2.0	—	37	150	—	190	
				4.5	—	17	30	—	38	
				6.0	—	15	26	—	32	
Input Capacitance	C_{IN}	DIR,G			—	5	10	—	10	pF
Bus Input Capacitance	C_{OUT}	An,Bn			—	13	—	—	—	
Power Dissipation Capacitance	$C_{PD}(1)$	TC74HC245A			—	39	—	—	—	
		TC74HC640A			—	37	—	—	—	

Note(1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation :

$$I_{CC}(\text{opr}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 8 \text{ (per bit)}$$

DIP 20PIN PACKAGE DIMENSIONS (DIP20-P-300-2.54A)

Unit in mm



SOP 20PIN (200mil BODY) PACKAGE DIMENSIONS (SOP20-P-300-1.27)

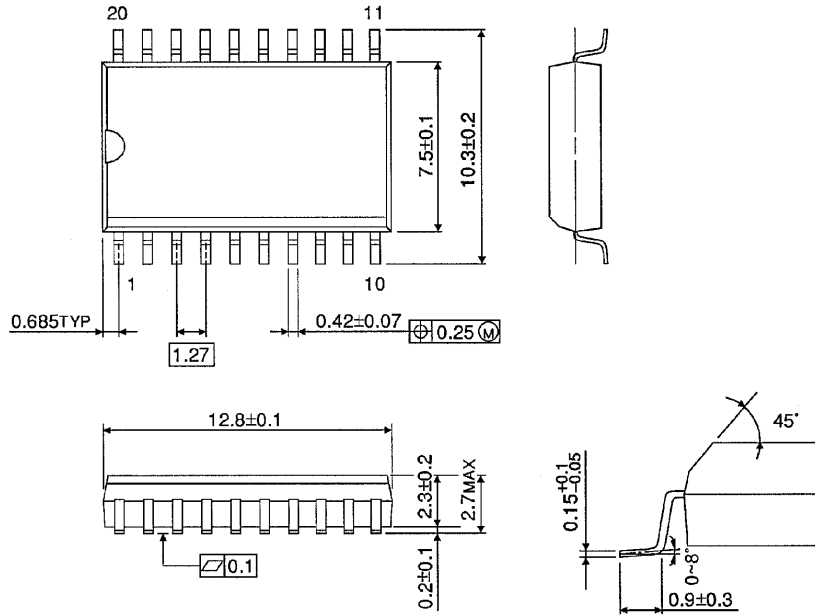
Unit in mm



SOP 20PIN (300mil BODY) PACKAGE DIMENSIONS (SOL20-P-300-1.27)

Unit in mm

(Note) This package is not available in Japan.



Weight : 0.46g (Typ.)

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