Features

- **Low Voltage and Standard Voltage Operation**
  - **5.0 (V_{CC} = 4.5V to 5.5V)**
  - **2.7 (V_{CC} = 2.7V to 5.5V)**
  - **2.5 (V_{CC} = 2.5V to 5.5V)**
- **User Selectable Internal Organization**
  - **1K: 128 x 8 or 64 x 16**
  - **2K: 256 x 8 or 128 x 16**
  - **4K: 512 x 8 or 256 x 16**
- **4-Wire Serial Interface**
- **Self-Timed Write Cycle (10 ms max)**
- **High Reliability**
  - **Endurance: 1 Million Write Cycles**
  - **Data Retention: 100 Years**
  - **ESD Protection: >4000V**
- **8-Pin PDIP and 8-Pin EIAJ SOIC Packages**

Description

The AT59C11/22/13 provides 1024/2048/4096 bits of serial EEPROM (Electrically Erasable Programmable Read Only Memory) organized as 64/128/256 words of 16 bits each, when the ORG Pin is connected to V_{CC} and 128/256/512 words of 8 bits each when it is tied to ground. The device is optimized for use in many industrial and commercial applications where low power and low voltage operation are essential. The AT59C11/22/13 is available in space saving 8-pin PDIP and 8-pin EIAJ SOIC packages.

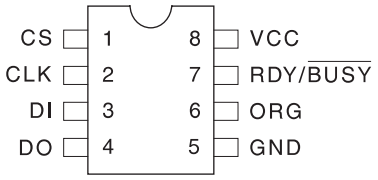
The AT59C11/22/13 is enabled through the Chip Select pin (CS), and accessed via a 4-wire serial interface consisting of Data Input (DI), Data Output (DO), and Clock (CLK). Upon receiving a READ instruction at DI, the address is decoded and the data is clocked out serially on the data output pin DO, the WRITE cycle is completely self-timed and no separate ERASE cycle is required before WRITE. The WRITE cycle is only enabled when the part is in the ERASE/WRITE ENABLE state. Ready/$\overline{\text{Busy}}$ status can be monitored upon completion of a programming operation by polling the Ready/$\overline{\text{Busy}}$ pin.

The AT59C11/22/13 is available in 5.0V ± 10%, 2.7V to 5.5V and 2.5V to 5.5V versions.

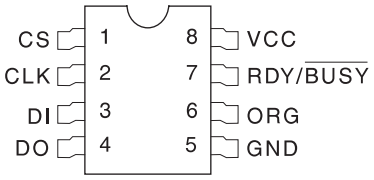
Pin Configurations

Pin Name	Function
CS	Chip Select
CLK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
V_{CC}	Power Supply
ORG	Internal Organization
RDY/$\overline{\text{BUSY}}$	Status Output

8-Pin PDIP



8-Pin SOIC



4-Wire Serial EEPROMs

1K (128 x 8 or 64 x 16)

2K (256 x 8 or 128 x 16)

4K (512 x 8 or 256 x 16)

AT59C11
AT59C22
AT59C13

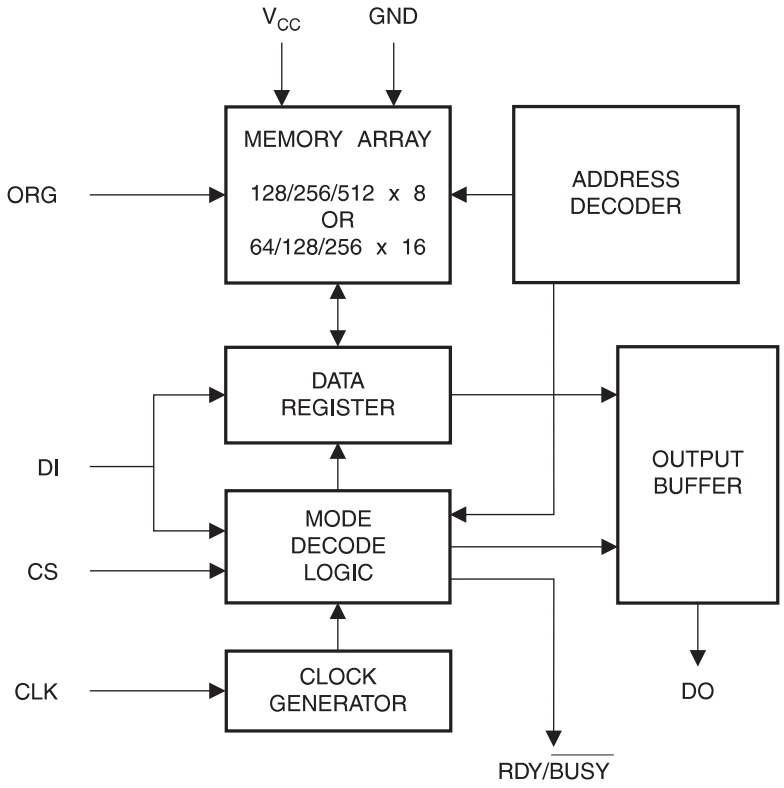
Rev. 0173K–07/98

Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-1.0V to +7.0V
Maximum Operating Voltage	6.25V
DC Output Current	5.0 mA

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Block Diagram(1)



Note: 1. When the ORG pin is connected to V_{CC}, the x 16 organization is selected. When it is connected to ground, the x 8 organization is selected. If the ORG pin is left unconnected, then an internal pullup device will select the x 16 organization.

Pin Capacitance[1]

Applicable over recommended operating range from T_A = 25°C, f = 1.0 MHz, V_{CC} = +5.0V (unless otherwise noted).

	Test Conditions	Max	Units	Conditions
C_{OUT}	Output Capacitance (DO)	5	pF	V_{OUT} = 0V
C_{IN}	Input Capacitance (CS, CLK, DI, RDY/$\overline{BUSY}$)	5	pF	V_{IN} = 0V

Note: 1. This parameter is characterized and is not 100% tested.

DC Characteristics

Applicable over recommended operating range from: T_{AI} = -40°C to +85°C, V_{CC} = +2.5V to +5.5V,
T_{AC} = 0°C to +70°C, V_{CC} = +2.5V to +5.5V (unless otherwise noted).

Symbol	Parameter	Test Condition		Min	Typ	Max	Units
V_{CC1}	Supply Voltage			1.8		5.5	V
V_{CC2}	Supply Voltage			2.5		5.5	V
V_{CC3}	Supply Voltage			2.7		5.5	V
V_{CC4}	Supply Voltage			4.5		5.5	V
I_{CC}	Supply Current	V_{CC} = 5.0V	READ at 1.0 MHz		0.5	2.0	mA
			WRITE at 1.0 MHz		0.5	2.0	mA
I_{SB1}	Standby Current	V_{CC} = 2.5V	CS = 0V		6.0	10.0	µA
I_{SB2}	Standby Current	V_{CC} = 2.7V	CS = 0V		6.0	10.0	µA
I_{SB3}	Standby Current	V_{CC} = 5.0V	CS = 0V		21.0	30.0	µA
I_{IL}	Input Leakage	V_{IN} = 0V to V_{CC}			0.1	1.0	µA
I_{OL}	Output Leakage	V_{IN} = 0V to V_{CC}			0.1	1.0	µA
V_{IL1}[1] V_{IH1}[1]	Input Low Voltage Input High Voltage	4.5V ≤ V_{CC} ≤ 5.5V		-0.6 2.0		0.8 V_{CC} + 1	V
V_{IL2}[1] V_{IH2}[1]	Input Low Voltage Input High Voltage	2.5V ≤ V_{CC} ≤ 2.7V		-0.6 V_{CC} x 0.7		V_{CC} x 0.3 V_{CC} + 1	V
V_{OL1} V_{OH1}	Output Low Voltage Output High Voltage	4.5V ≤ V_{CC} ≤ 5.5V	I_{OL} = 2.1 mA I_{OH} = 0.4 mA	 2.4		0.4	V
V_{OL2} V_{OH2}	Output Low Voltage Output High Voltage	2.5V ≤ V_{CC} ≤ 2.7V	I_{OL} = 0.15 mA I_{OH} = -0.1 mA	 V_{CC} - 0.2		0.2	V

Note: 1. V_{IL} min and V_{IH} max are reference only and are not tested.

AC Characteristics

Applicable over recommended operating range from T_A = -40°C to +85°C, V_{CC} = +2.5V to +5.5V, CL = 1 TTL Gate and 100 pF (unless otherwise noted).

Symbol	Parameter	Test Condition		Min	Typ	Max	Units
f_{CLK}	CLK Clock Frequency	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $2.5V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$		0 0 0 0		1 1 0.5 0.25	MHz
t_{CKH}	CLK High Time	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $2.5V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$		250 250 500 1000			ns
t_{CKL}	CLK Low Time	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $2.5V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$		250 250 500 1000			ns
t_{CS}	Minimum CS Low Time	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $2.5V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$		250 250 500 1000			ns
t_{CSS}	CS Setup Time	Relative to SK	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $2.5V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$	50 50 100 200			ns
t_{DIS}	DI Setup Time	Relative to SK	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $2.5V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$	100 100 200 400			ns
t_{CSH}	CS Hold Time	Relative to SK		0			ns
t_{DIH}	DI Hold Time	Relative to SK	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $2.5V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$	100 100 200 400			ns
t_{PD1}	Output Delay to ‘1’	AC Test	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $2.5V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$			250 250 500 1000	ns
t_{PD0}	Output Delay to ‘0’	AC Test	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $2.5V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$			250 250 500 1000	ns
t_{RBD}	RDY/$\overline{BUSY}$ Delay to Status Valid	AC Test	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $2.5V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$			250 250 500 1000	ns
t_{CZ}	CS to DO in High Impedance	AC Test CS = V_{IL}	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$ $2.5V \le V_{CC} \le 5.5V$ $1.8V \le V_{CC} \le 5.5V$			100 100 200 400	ns
t_{WC}	Write Cycle Time			0.1		10	ms
Endurance[1]	5.0V, 25°C, Page Mode			1M			Write Cycles

Note: 1. This paramter is characterized and is not 100% tested.

Instruction Set for the AT59C11

Instruction	SB	Op Code	Address		Data		Comments
			x 8	x 16	x 8	x 16	
READ	1	10XX	A_6 - A_0	A_5 - A_0			Reads data stored in memory, at specified address.
EWEN	1	0011	XXXXXXX	XXXXXX			Write enable must precede all programming modes.
WRITE	1	X1XX	A_6 - A_0	A_5 - A_0	D_7 - D_0	D_{15} - D_0	Writes memory location A_n - A_0.
ERAL	1	0010	XXXXXXX	XXXXXX			Erases all memory locations. Valid only at V_{CC} = 4.5V to 5.5V.
WRAL	1	0001	XXXXXXX	XXXXXX	D_7 - D_0	D_{15} - D_0	Writes all memory locations. Valid only at V_{CC} = 4.5V to 5.5V.
EWDS	1	0000	XXXXXXX	XXXXXX			Disables all programming instructions.

Instruction Set for the AT59C22

Instruction	SB	Op Code	Address		Data		Comments
			x 8	x 16	x 8	x 16	
READ	1	10XX	A_7 - A_0	A_6 - A_0			Reads data stored in memory, at specified address.
EWEN	1	0011	XXXXXXXX	XXXXXXX			Write enable must precede all programming modes.
WRITE	1	X1XX	A_7 - A_0	A_6 - A_0	D_7 - D_0	D_{15} - D_0	Writes memory location A_n - A_0.
ERAL	1	0010	XXXXXXXX	XXXXXXX			Erases all memory locations. Valid only at V_{CC} = 4.5V to 5.5V.
WRAL	1	0001	XXXXXXXX	XXXXXXX	D_7 - D_0	D_{15} - D_0	Writes all memory locations. Valid when V_{CC} = 5.0V ± 10% and Disable Register cleared.
EWDS	1	0000	XXXXXXXX	XXXXXXX			Disables all programming instructions.

Instruction Set for the AT59C13

Instruction	SB	Op Code	Address		Data		Comments
			x 8	x 16	x 8	x 16	
READ	1	10XX	A_8 - A_0	A_7 - A_0			Reads data stored in memory, at specified address.
EWEN	1	0011	XXXXXXXXX	XXXXXXXX			Write enable must precede all programming modes.
WRITE	1	X1XX	A_8 - A_0	A_7 - A_0	D_7 - D_0	D_{15} - D_0	Writes memory location A_n - A_0.
ERAL	1	0010	XXXXXXXXX	XXXXXXXX			Erases all memory locations. Valid only at V_{CC} = 4.5V to 5.5V.
WRAL	1	0001	XXXXXXXXX	XXXXXXXX	D_7 - D_0	D_{15} - D_0	Writes all memory locations. Valid when V_{CC} = 5.0V ± 10% and Disable Register cleared.
EWDS	1	0000	XXXXXXXXX	XXXXXXXX			Disables all programming instructions.

Functional Description

The AT59C11/22/13 are accessed via a simple and versatile 4-wire serial communication interface. Device operation is controlled by six instructions issued by the host processor. **A valid instruction starts with a rising edge of CS** and consists of a Start Bit (logic '1') followed by the appropriate Op Code and the desired memory Address location.

READ (READ): The Read (READ) instruction contains the Address code for the memory location to be read. After the instruction and address are decoded, data from the selected memory location is available at the serial output pin DO. Output data changes are synchronized with the rising edges of serial clock CLK. It should be noted that a dummy bit (logic '0') precedes the 8- or 16-bit data output string.

ERASE/WRITE (EWEN): To assure data integrity, the part automatically goes into the Erase/Write Disable (EWDS) state when power is first applied. An Erase/Write Enable (EWEN) instruction must be executed first before any programming instructions can be carried out. Please note that once in the Erase/Write Enable state, programming remains enabled until an Erase/Write Disable (EWDS) instruction is executed or V_{CC} power is removed from the part.

WRITE (WRITE): The Write (WRITE) instruction contains the 8 or 16 bits of data to be written into the specified memory location. The self-timed programming cycle, t_{WP}, starts after the last bit of data is received at serial data input pin DI. The Ready/$\overline{\text{Busy}}$ status of the AT59C11/22/13 can be determined by polling the RDY/$\overline{\text{BUSY}}$ pin. A logic '0' at RDY/$\overline{\text{BUSY}}$ indicates that programming is still in progress. A logic '1' indicates that the memory location at the specified address has been written with the data pattern contained in the instruction and the part is ready for further instructions.

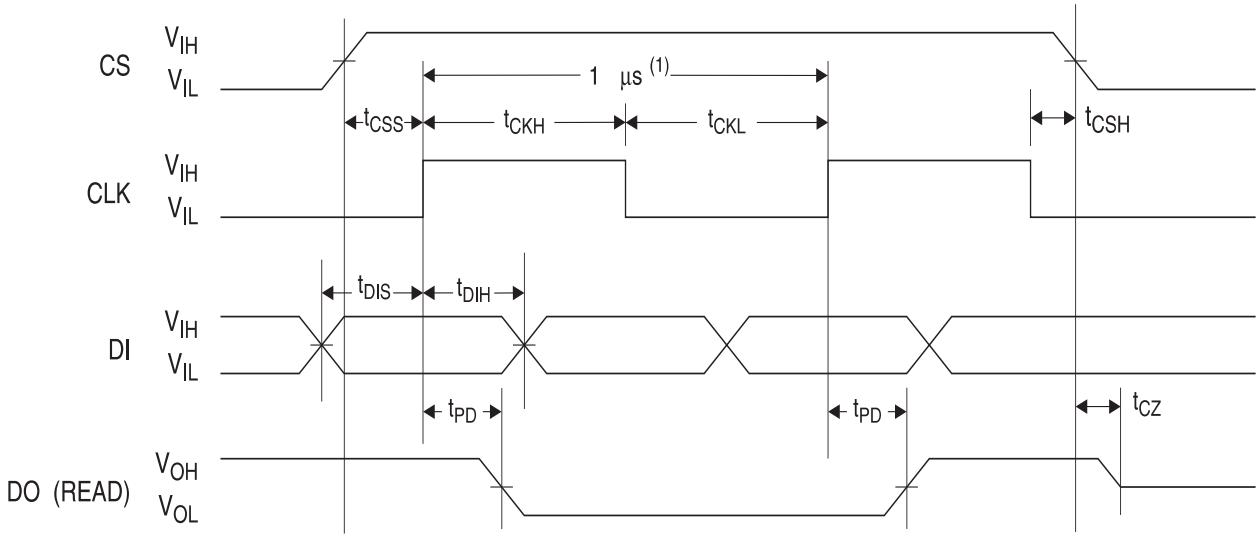
ERASE ALL (ERAL): The Erase All (ERAL) instruction programs every bit in the memory array to the logic '1' state and is primarily used for testing purposes. The Ready/$\overline{\text{Busy}}$ status of the AT59C11/22/13 can be determined by polling the RDY/$\overline{\text{BUSY}}$ pin. The ERAL instruction is valid only at V_{CC} = 5.0V ± 10%.

WRITE ALL (WRAL): The Write All (WRAL) instruction programs all memory locations with the data patterns specified in the instruction. The Ready/$\overline{\text{Busy}}$ status of the AT59C11/22/13 can be determined by polling the RDY/$\overline{\text{BUSY}}$ pin. The WRAL instruction is valid only at V_{CC} = 5.0V ± 10%.

ERASE/WRITE DISABLE (EWDS): To protect against accidental data disturb, the Erase/Write Disable (EWDS) instruction disables all programming modes and should be executed after all programming operations. The operation of the READ instruction is independent of both the EWEN and EWDS instructions and can be executed at any time.

Timing Diagrams

Synchronous Data Timing

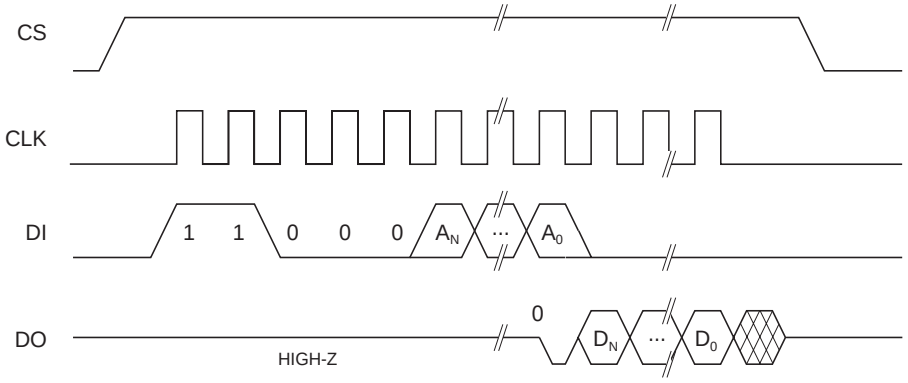


Note: 1. This is the minimum CLK period.

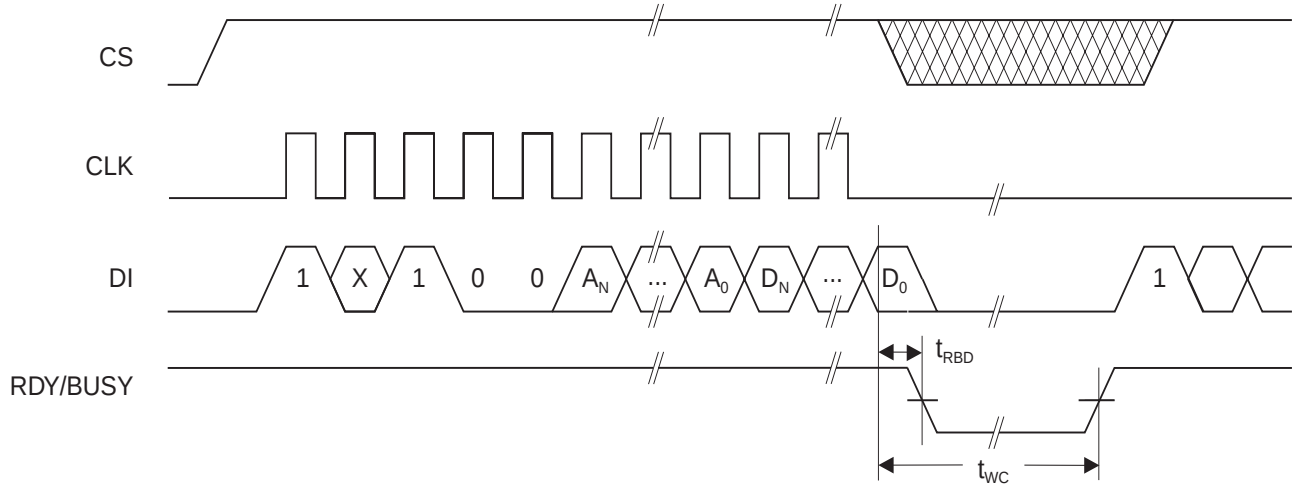
Organization Key for Timing Diagrams

	Density 1K		Density 2K		Density 4K	
I/O	**x 8**	**x 16**	**x 8**	**x 16**	**x 8**	**x 16**
A_N	A_6	A_5	A_7	A_6	A_8	A_7
D_N	D_7	D_{15}	D_7	D_{15}	D_7	D_{15}

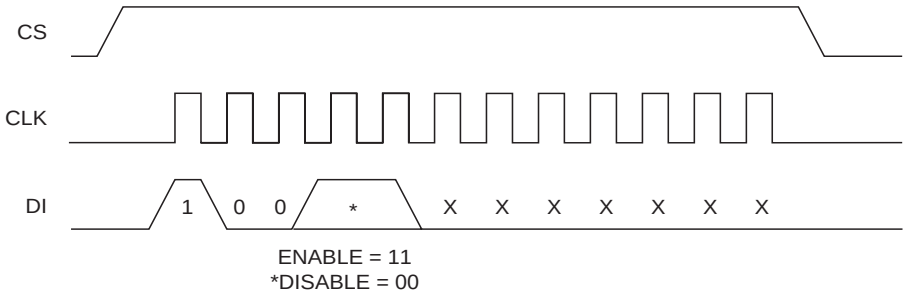
READ Timing



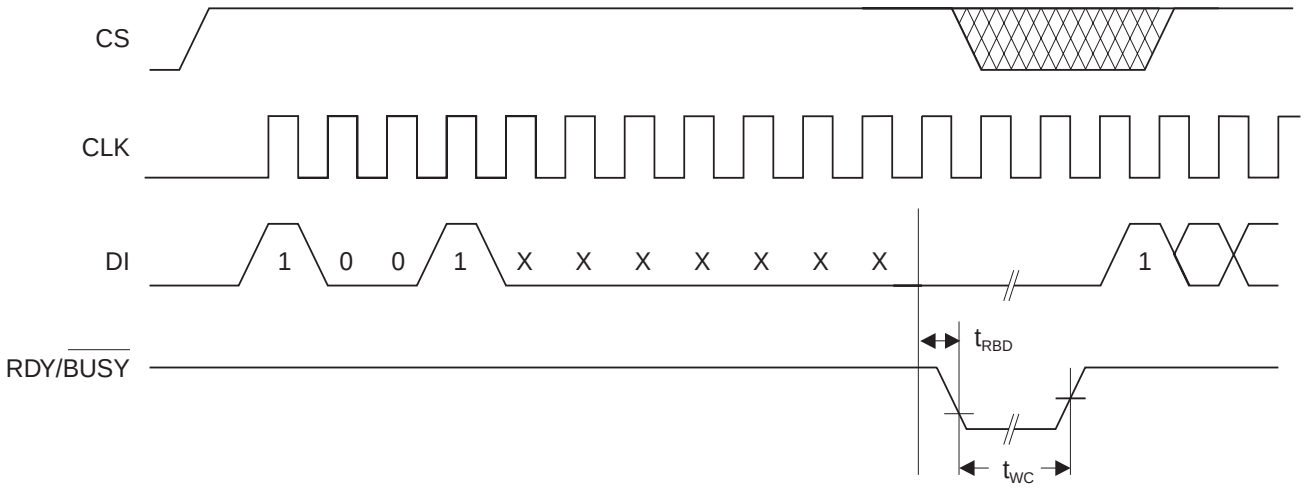
WRITE Timing



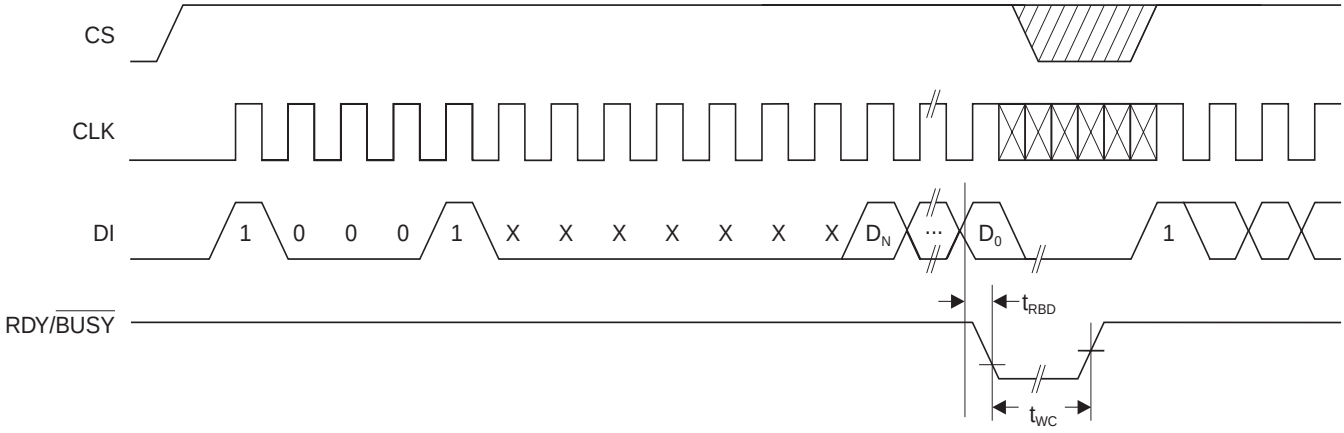
EWEN/EWDS Timing



ERAL Timing



WRAL Timing



AT59C11 Ordering Information

t_{WC} (max) (ms)	I_{CC} (max) (μA)	I_{SB} (max) (μA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	2000	30.0	1000	AT59C11-10PC AT59C11W-10SC	8P3 8S2	Commercial (0°C to 70°C)
		30.0	1000	AT59C11-10PI AT59C11W-10SI	8P3 8S2	Industrial (-40°C to 85°C)
10	800	10.0	1000	AT59C11-10PC-2.7 AT59C11W-10SC-2.7	8P3 8S2	Commercial (0°C to 70°C)
		10.0	1000	AT59C11-10PI-2.7 AT59C11W-10SI-2.7	8P3 8S2	Industrial (-40°C to 85°C)
10	600	10.0	500	AT59C11-10PC-2.5 AT59C11W-10SC-2.5	8P3 8S2	Commercial (0°C to 70°C)
		10.0	500	AT59C11-10PI-2.5 AT59C11W-10SI-2.5	8P3 8S2	Industrial (-40°C to 85°C)

Package Type	
8P3	8-Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S2	8-Lead, 0.200" Wide, Plastic Gull Wing Small Outline (EIAJ SOIC)
Options	
Blank	Standard Device (4.5V to 5.5V)
-2.7	Low-Voltage (2.7V to 5.5V)
-2.5	Low-Voltage (2.5V to 5.5V)

AT59C22 Ordering Information

t_{WC} (max) (ms)	I_{CC} (max) (μA)	I_{SB} (max) (μA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	2000	30.0	1000	AT59C22-10PC AT59C22W-10SC	8P3 8S2	Commercial (0°C to 70°C)
		30.0	1000	AT59C22-10PI AT59C22W-10SI	8P3 8S2	Industrial (-40°C to 85°C)
10	800	10.0	1000	AT59C22-10PC-2.7 AT59C22W-10SC-2.7	8P3 8S2	Commercial (0°C to 70°C)
		10.0	1000	AT59C22-10PI-2.7 AT59C22W-10SI-2.7	8P3 8S2	Industrial (-40°C to 85°C)
10	600	10.0	500	AT59C22-10PC-2.5 AT59C22W-10SC-2.5	8P3 8S2	Commercial (0°C to 70°C)
		10.0	500	AT59C22-10PI-2.5 AT59C22W-10SI-2.5	8P3 8S2	Industrial (-40°C to 85°C)

Package Type	
8P3	8-Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S2	8-Lead, 0.200" Wide, Plastic Gull Wing Small Outline (EIAJ SOIC)
Options	
Blank	Standard Device (4.5V to 5.5V)
-2.7	Low-Voltage (2.7V to 5.5V)
-2.5	Low-Voltage (2.5V to 5.5V)

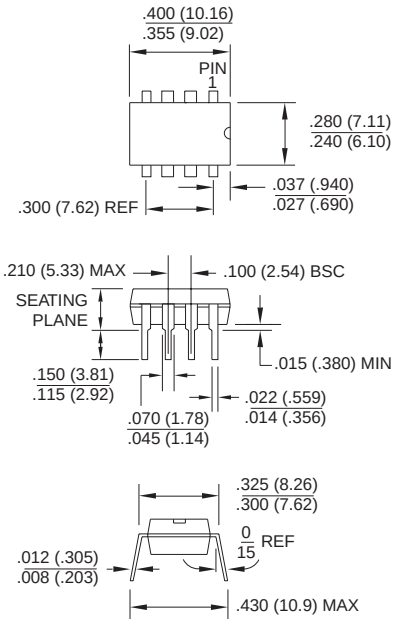
AT59C13 Ordering Information

t_{WC} (max) (ms)	I_{CC} (max) (μA)	I_{SB} (max) (μA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	2000	30.0	1000	AT59C13-10PC AT59C13W-10SC	8P3 8S2	Commercial (0°C to 70°C)
		30.0	1000	AT59C13-10PI AT59C13W-10SI	8P3 8S2	Industrial (-40°C to 85°C)
10	800	10.0	1000	AT59C13-10PC-2.7 AT59C13W-10SC-2.7	8P3 8S2	Commercial (0°C to 70°C)
		10.0	1000	AT59C13-10PI-2.7 AT59C13W-10SI-2.7	8P3 8S2	Industrial (-40°C to 85°C)
10	600	10.0	500	AT59C13-10PC-2.5 AT59C13W-10SC-2.5	8P3 8S2	Commercial (0°C to 70°C)
		10.0	500	AT59C13-10PI-2.5 AT59C13W-10SI-2.5	8P3 8S2	Industrial (-40°C to 85°C)

Package Type	
8P3	8-Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S2	8-Lead, 0.200" Wide, Plastic Gull Wing Small Outline (EIAJ SOIC)
Options	
Blank	Standard Device (4.5V to 5.5V)
-2.7	Low-Voltage (2.7V to 5.5V)
-2.5	Low-Voltage (2.5V to 5.5V)

Packaging Information

8P3, 8-Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
Dimensions in Inches and (Millimeters)
JEDEC STANDARD MS-001 BA



8S2, 8-Lead, 0.200" Wide, Plastic Gull Wing Small Outline (EIAJ SOIC)
Dimensions in Inches and (Millimeters)