NPN
MJ14002*
PNP
MJ14001
MJ14003*

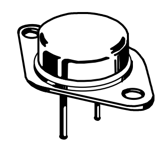
*Motorola Preferred Device

High-Current Complementary Silicon Power Transistors

. . . designed for use in high–power amplifier and switching circuit applications,

- High Current Capability — I_C Continuous = 60 Amperes
- DC Current Gain — h_{FE} = 15–100 @ I_C = 50 Adc
- Low Collector–Emitter Saturation Voltage — $V_{CE(sat)}$ = 2.5 Vdc (Max) @ I_C = 50 Adc

60 AMPERES
COMPLEMENTARY
SILICON
POWER TRANSITORS
60–80 VOLTS
300 WATTS



CASE 197A–05
TO–204AE (TO–3)

MAXIMUM RATINGS

Rating	Symbol	MJ14001	MJ14002 MJ14003	Unit
Collector–Emitter Voltage	V_{CEO}	60	80	Vdc
Collector Base Voltage	V_{CBO}	60	80	Vdc
Emitter–Base Voltage	V_{EBO}	5		Vdc
Collector Current — Continuous	I_C	60		Adc
Base Current — Continuous	I_B	15		Adc
Emitter Current — Continuous	I_E	75		
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	300 17		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.584	°C/W

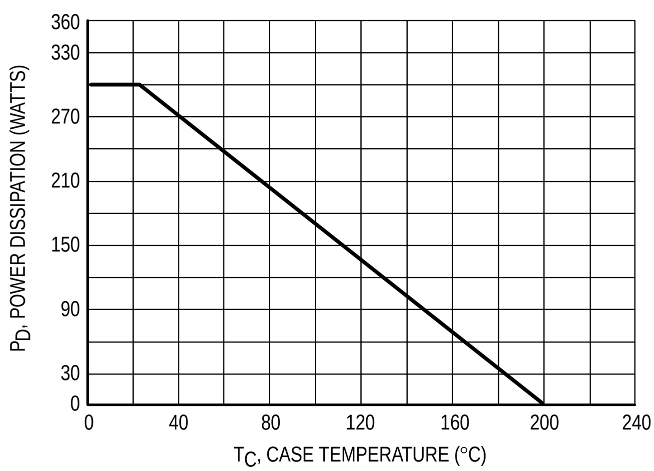


Figure 1. Power Derating

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 2

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 200 mAdc, I_B = 0)	MJ14001		60	—	
	MJ14002, MJ14003		80	—	
Collector Cutoff Current		I_{CEO}			mA
(V_{CE} = 30 Vdc, I_B = 0)	MJ14001		—	1.0	
(V_{CE} = 40 Vdc, I_B = 0)	MJ14402, MJ14003		—	1.0	
Collector Cutoff Current		I_{CEX}			mA
(V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 V)	MJ14001		—	1.0	
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 V)	MJ14002, MJ14003		—	1.0	
Collector Cutoff Current		I_{CBO}			mA
(V_{CB} = 60 Vdc, I_E = 0)	MJ14001		—	1.0	
(V_{CB} = 80 Vdc, I_E = 0)	MJ14002, MJ14003		—	1.0	
Emitter Cutoff Current (V_{BE} = 5 Vdc, I_C = 0)		I_{EBO}	—	1.0	mA
ON CHARACTERISTICS					
DC Current Gain (1)		h_{FE}			—
(I_C = 25 Adc, V_{CE} = 3.0 V)			30	—	
(I_C = 50 Adc, V_{CE} = 3.0 V)			15	100	
(I_C = 60 Adc, V_{CE} = 3.0 V)			5	—	
Collector–Emitter Saturation Voltage (1)		$V_{CE(sat)}$			Vdc
(I_C = 25 Adc, I_B = 2.5 Adc)			—	1	
(I_C = 50 Adc, I_B = 5.0 Adc)			—	2.5	
(I_C = 60 Adc, I_B = 12 Adc)			—	3	
Base–Emitter Saturation Voltage (1)		$V_{BE(sat)}$			Vdc
(I_C = 25 Adc, I_B = 2.5 Adc)			—	2	
(I_C = 50 Adc, I_B = 5.0 Adc)			—	3	
(I_C = 60 Adc, I_B = 12 Adc)			—	4	
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)		C_{ob}	—	2000	pF

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.

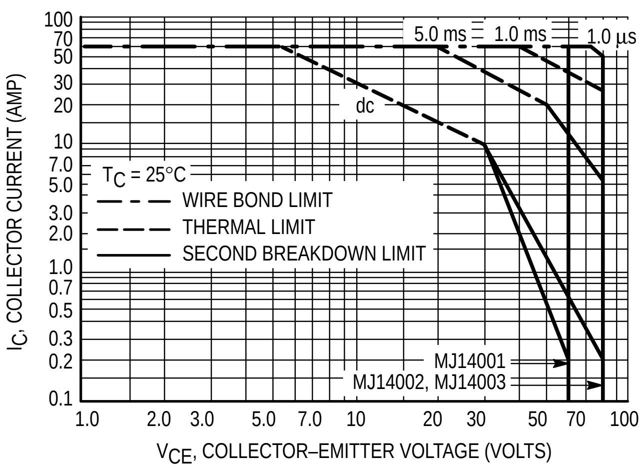


Figure 2. Maximum Rated Forward Biased Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C – V_{CE} limits of the transistor that must be observed for reliable operation: i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on $T_{J(pk)}$ = 200°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)}$ ≤ 200°C. $T_{J(pk)}$ may be calculated from the data in Figure 13. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

TYPICAL ELECTRICAL CHARACTERISTICS

NPN
MJ14002

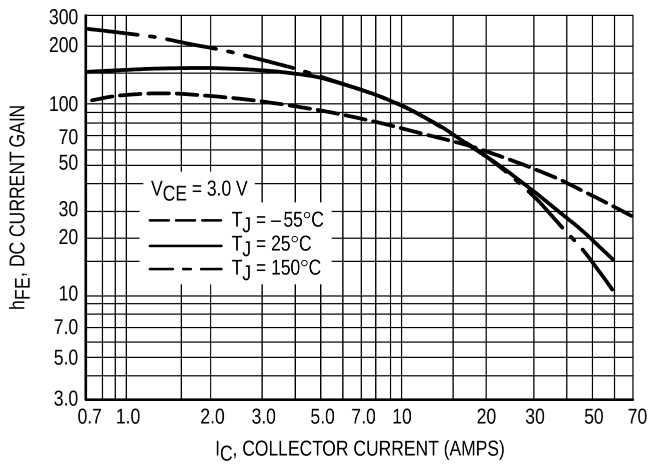


Figure 3. DC Current Gain

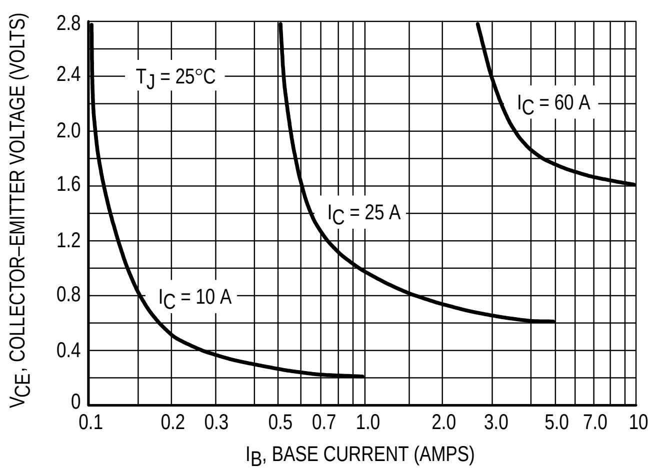


Figure 5. Collector Saturation Region

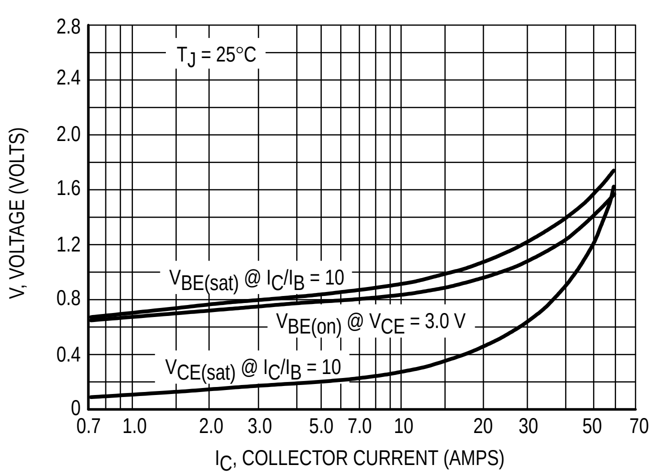


Figure 7. “On” Voltages

PNP
MJ14001, MJ14003

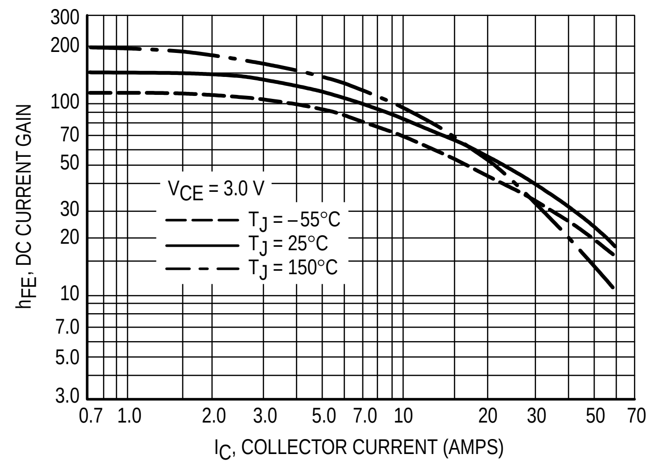


Figure 4. DC Current Gain

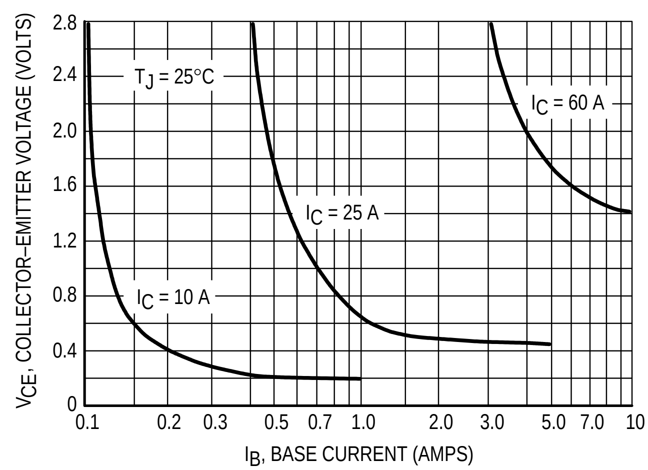


Figure 6. Collector Saturation Region

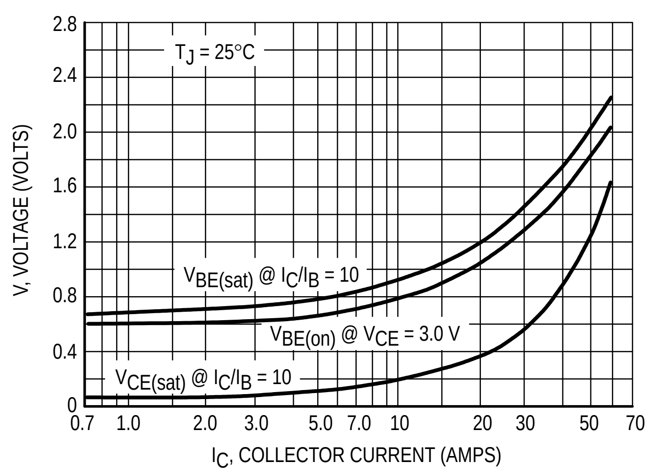


Figure 8. “On” Voltages

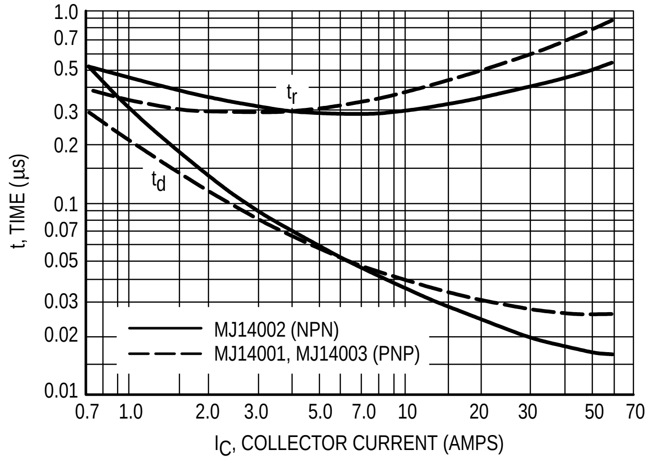


Figure 9. Turn–On Switching Times

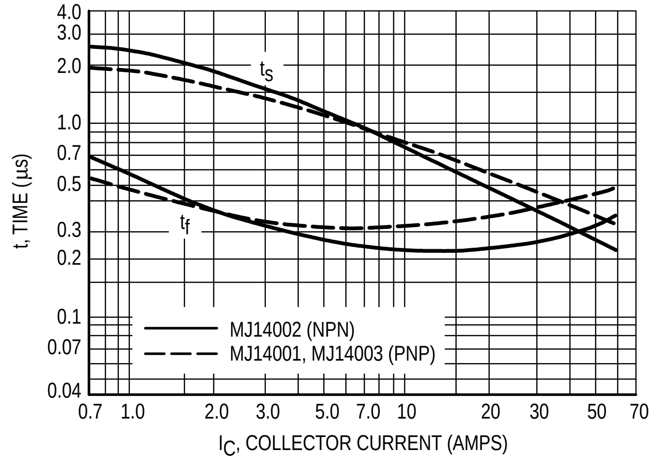


Figure 10. Turn–Off Switching Times

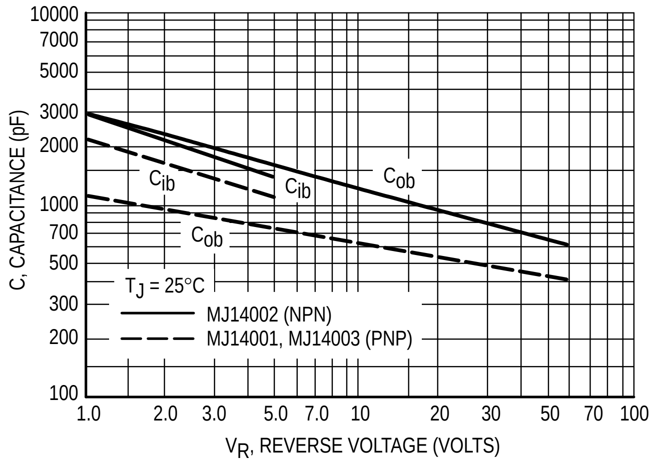
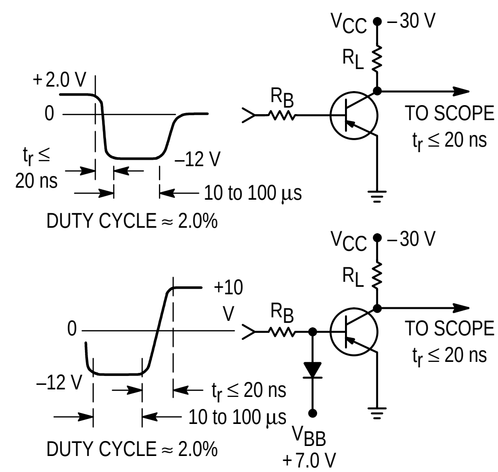


Figure 11. Capacitance Variation



FOR CURVES OF FIGURES 3 & 6, R_B & R_L ARE VARIED.
INPUT LEVELS ARE APPROXIMATELY AS SHOWN.
FOR NPN CIRCUITS, REVERSE ALL POLARITIES.

Figure 12. Switching Test Circuit

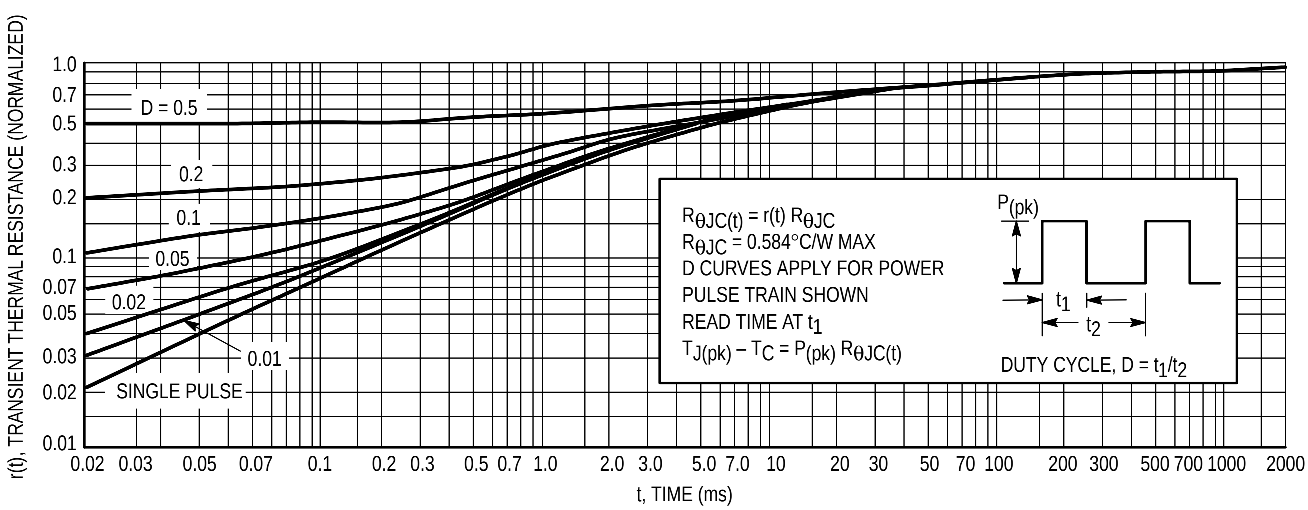
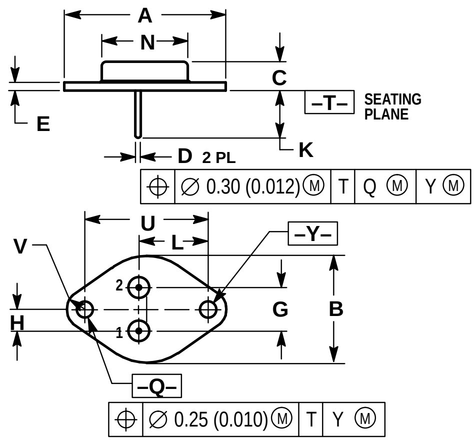


Figure 13. Thermal Response

PACKAGE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.530 REF		38.86 REF	
B	0.990	1.050	25.15	26.67
C	0.250	0.335	6.35	8.51
D	0.057	0.063	1.45	1.60
E	0.060	0.070	1.53	1.77
G	0.430 BSC		10.92 BSC	
H	0.215 BSC		5.46 BSC	
K	0.440	0.480	11.18	12.19
L	0.665 BSC		16.89 BSC	
N	0.760	0.830	19.31	21.08
Q	0.151	0.165	3.84	4.19
U	1.187 BSC		30.15 BSC	
V	0.131	0.188	3.33	4.77

STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

CASE 197A–05
TO–204AE (TO–3)
ISSUE J

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