FAIRCHILD
A Schlumberger Company

μA96173 • μA96175 Quad Differential Line Receivers

Linear Division Interface Products

Description

The μA96173 and μA96175 are high speed quad differential line receivers designed to meet EIA Standard RS-485. The devices have three-state outputs and are optimized for balanced multipoint data bus transmission at rates up to 10 Mbps. The receivers feature high input impedance, input hysteresis for increased noise immunity, and input sensitivity of 200 mV over a common mode input voltage range of −12 V to +12 V. The receivers are therefore suitable for multipoint applications in noisy environments. The μA96173 features an active high and active low Enable, common to all four receivers. The μA96175 features separate active high Enables for each receiver pair. Compatible RS-485 drivers, transceivers, and repeaters are also offered by Fairchild and are designed to provide optimum bus performance. The respective device types are μA96172/96174, μA96176 and μA96177/96178.

- **Meets EIA Standard RS-485, RS-422A, RS-423A**
- **Designed For Multipoint Bus Applications**
- **Three-State Outputs**
- **Common Mode Input Voltage Range: −12 V To +12 V**
- **Operates From Single +5.0 V Supply**
- **Input Sensitivity Of ±200 mV Over Common Mode Range**
- **Input Hysteresis Of 50 mV Typical**
- **High Input Impedance**
- **Fail-Safe Input/Output Features Drive Output HIGH When Input Is Open**
- **μA96173/96175 Are Lead And Function Compatible With SN75173/75175 Or The AM26LS32/MC3486 Respectively.**

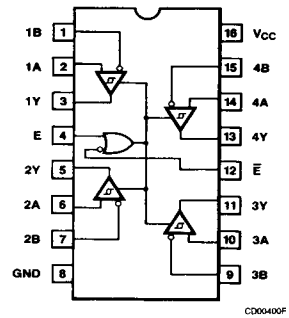
Function Table (Each Receiver) μA96173

Differential Inputs	Enables		Outputs
A − B	E	$\overline{E}$	V
$V_{ID} > 0.2$ V	H	X	H
	X	L	H
−0.2 V < V_{ID} < 0.2 V	H	X	?
	X	L	?
$V_{ID} < -0.2$ V	H	X	L
	X	L	L
X	L	H	Z

H = High Level
L = Low Level
? = Indeterminate
X = Immaterial
Z = High Impedance (off)

Connection Diagram 16-Lead DIP (Top View)

μA96173



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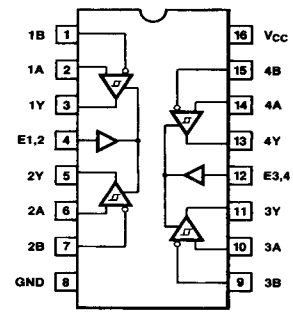
μA96175



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Order Information

Device Code	Package Code	Package Description
μA96173DC	7B	Ceramic DIP
μA96173PC	9B	Molded DIP
μA96175DC	7B	Ceramic DIP
μA96175PC	9B	Molded DIP

Function Table (Each Receiver) μA96175

Differential Inputs A − B	Enable	Output Y
$V_{ID} \geq 0.2$ V	H	H
−0.2 V < V_{ID} < 0.2 V	H	?
$V_{ID} \leq -0.2$ V	H	L
X	L	Z

Absolute Maximum Ratings

Storage Temperature Range	
Ceramic DIP	−65°C to +175°C
Molded DIP	−65°C to +150°C
Operating Temperature Range	0°C to +70°C
Lead Temperature	
Ceramic DIP (soldering, 60 s)	300°C
Molded DIP (soldering, 10 s)	265°C
Internal Power Dissipation[1,2]	
16L-Ceramic DIP	1.50 W
16L-Molded DIP	1.04 W
Supply Voltage[3]	7.0 V
Input Voltage, A or B Inputs	±25 V
Differential Input Voltage	±25 V
Enable Input Voltage	7.0 V
Low Level Output Current	50 mA

Notes
1. $T_{J\ Max}$ = 150°C for the Molded DIP, and 175°C for the Ceramic DIP.
2. Ratings apply to ambient temperature at 25°C. Above this temperature, derate the 16L-Ceramic DIP at 10 mW/°C, and the 16L-Molded DIP at 8.3 mW/°C.
3. All voltages are with respect to network ground terminal.

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Recommended Operating Conditions

Symbol	Characteristic	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	4.75	5.0	5.25	V
V_{CM}	Common Mode Input Voltage	−12[1]		+12	V
V_{ID}	Differential Input Voltage[2]	−12		+12	V
I_{OH}	Output Current HIGH			−400	μA
I_{OL}	Output Current LOW			16	mA
T_A	Operating Temperature	0	25	70	°C

Notes
1. The algebraic convention, where the less positive (more negative) limit is designated minimum, is used in this data sheet for common mode input voltage and threshold voltage levels only.
2. Differential input/output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.

μA96173, μA96175

Electrical Characteristics Over recommended temperature, common mode input voltage, and supply voltage ranges, unless otherwise specified.

Symbol	Characteristic	Condition	Min	Typ[1]	Max	Unit
V_{TH}	Differential-Input High Threshold Voltage	V_O = 2.7 V, I_O = −0.4 mA			0.2	V
V_{TL}	Differential-Input Low Threshold Voltage	V_O = 0.5 V, I_O = 16 mA	−0.2[2]			V
$V_{T+} - V_{T-}$	Hysteresis[3]	V_{CM} = 0 V		50		mV
V_{IH}	Enable Input Voltage HIGH		2.0			V

μA96173, μA96175 (Cont.)

Electrical Characteristics Over recommended temperature, common mode input voltage, and supply voltage ranges, unless otherwise specified.

Symbol	Characteristic	Condition		Min	Typ[1]	Max	Unit
V_{IL}	Enable Input Voltage LOW					0.8	V
V_{IC}	Enable Input Clamp Voltage	$I_I = -18$ mA				−1.5	V
V_{OH}	Output Voltage HIGH	$V_{ID} = 200$ mV, $I_{OH} = -400$ μA				2.7	V
V_{OL}	Output Voltage LOW	$V_{ID} = -200$ mV	$I_{OL} = 8.0$ mA			0.45	V
			$I_{OL} = 16$ mA			0.50	
I_{OZ}	High-Impedance State Output	$V_O = 0.4$ V to 2.4 V				±20	μA
I_I	Line Input Current[4]	Other Input = 0 V	$V_I = 12$ V			1.0	mA
			$V_I = -7.0$ V			−0.8	
I_{IH}	Enable Input Current HIGH	$V_{IH} = 2.7$ V				20	μA
I_{IL}	Enable Input Current LOW	$V_{IL} = 0.4$ V				−100	μA
R_I	Input Resistance				12		kΩ
I_{OS}	Short Circuit Output Current			−15		−85	mA
I_{CC}	Supply Current	Outputs Disabled				75	mA

Switching Characteristics $V_{CC} = 5.0$ V, $T_A = 25°C$

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
t_{PLH}	Propagation Delay Time, Low to High Level Output	$V_{ID} = -2.5$ V to 2.5 V, $C_L = 15$ pF, Fig. 1		15	25	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output			15	25	ns
t_{PZH}	Output Enable Time to High Level	$C_L = 15$ pF, Fig. 2		15	22	ns
t_{PZL}	Output Enable Time to Low Level	$C_L = 15$ pF, Fig. 3		15	22	ns
t_{PHZ}	Output Disable Time from High Level	$C_L = 5.0$ pF, Fig. 2		14	30	ns
t_{PLZ}	Output Disable Time from Low Level	$C_L = 5.0$ pF, Fig. 3		24	40	ns

Notes

1. All Typical values are at $V_{CC} = 5.0$ V, $T_A = 25°C$.
2. The algebraic convention, where the less positive (more negative) limit is designated minimum, is used in this data sheet for common mode input voltage and threshold voltage levels only.
3. Hysteresis is the difference between the positive-going input threshold voltage, $V_{T}+$, and the negative-going input threshold voltage, $V_{T}-$.
4. Refer to EIA standard RS-485 for exact conditions.

Parameter Measurement Information

Figure 1 t_{PLH}, t_{PHL} (Note 3)

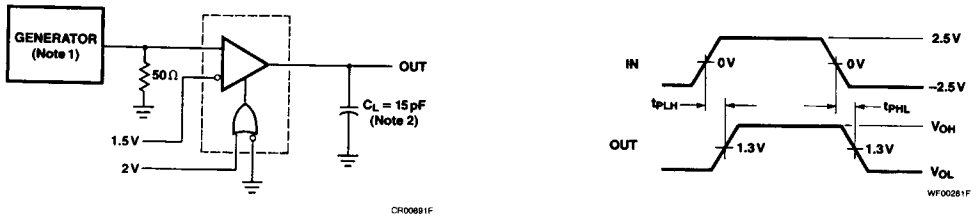


Figure 2 t_{PHZ}, t_{PZH} (Note 3)

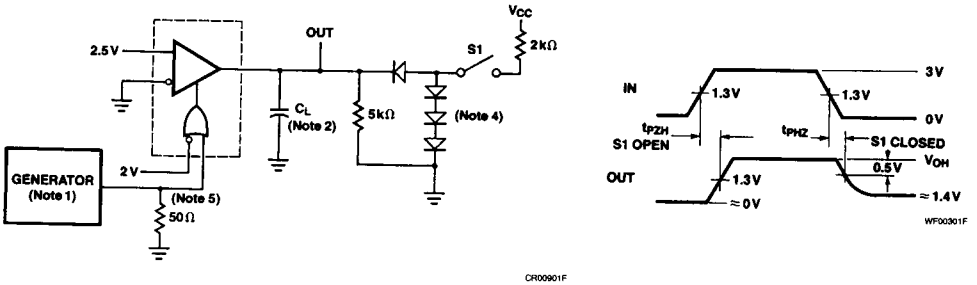
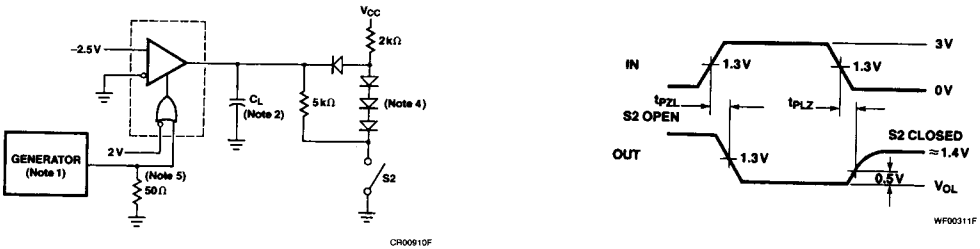


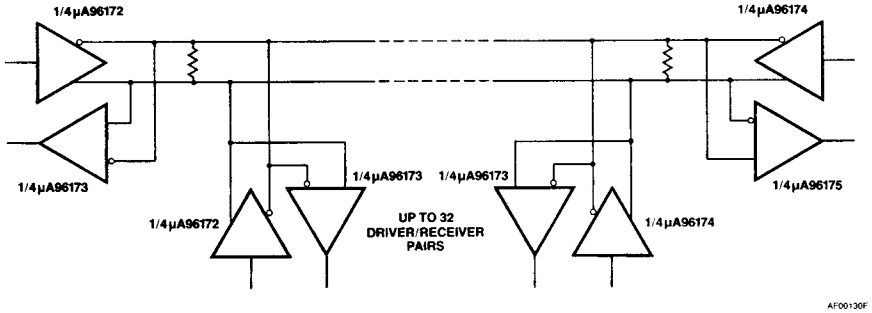
Figure 3 t_{PZL}, t_{PLZ} (Note 3)



Notes

1. The input pulse is supplied by a generator having the following characteristics: PRR = 1.0 MHz, 50% duty cycle, $t_r \leqslant 6.0$ ns, $t_f \leqslant 6.0$ ns, $Z_O = 50\ \Omega$.
2. C_L includes probe and jig capacitance.
3. μA96173 with active high and active low Enables is shown here. μA96175 has active high Enable only.
4. All diodes are 1N916 or equivalent.
5. To test the active low Enable $\overline{E}$ of μA96173, ground E and apply an inverted input waveform to $\overline{E}$. μA96175 has active high Enable only.

Typical Application



Note
The line length should be terminated at both ends in its characteristic impedance.
Stub lengths off the main line should be kept as short as possible.